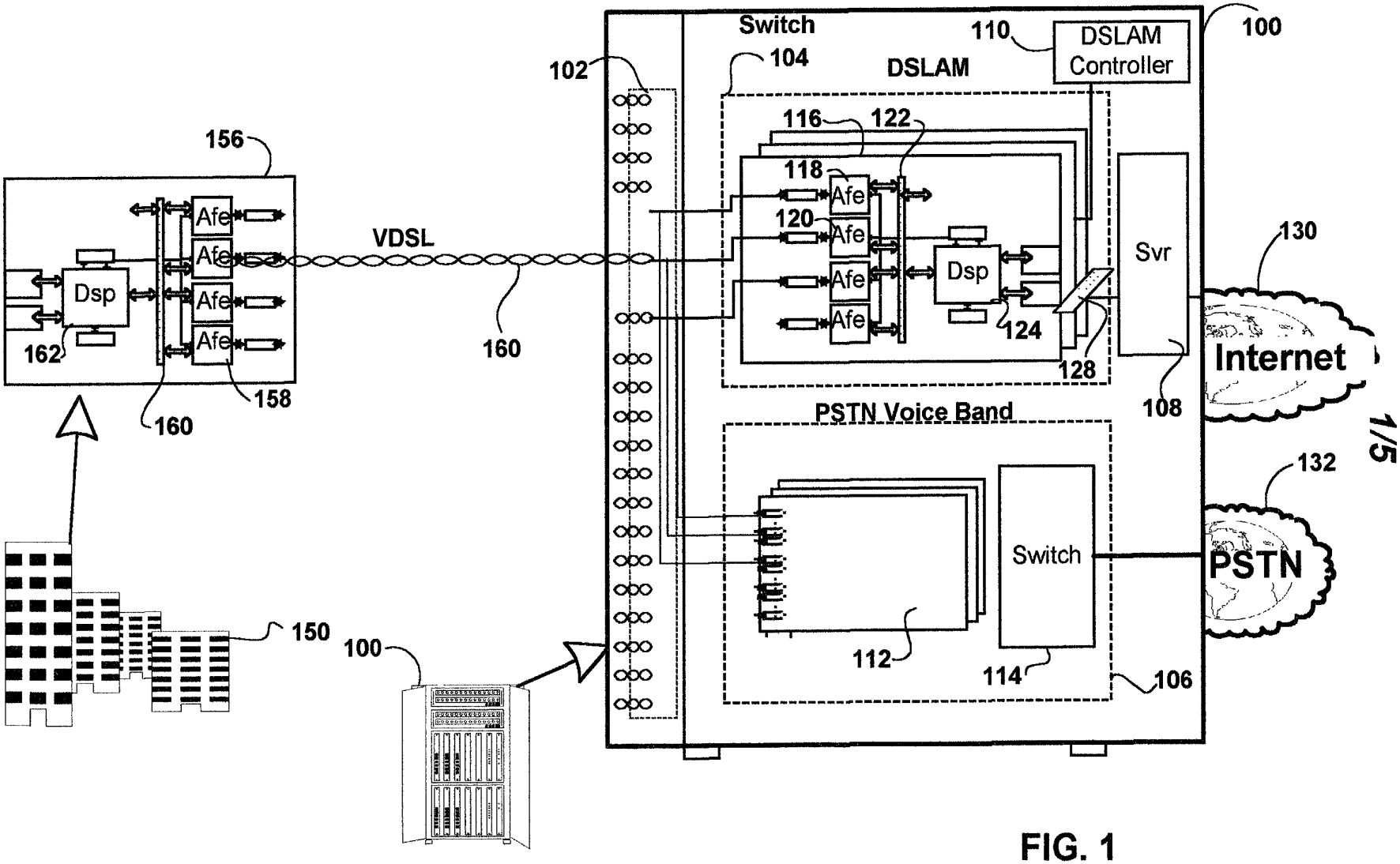
Switch
110
DSLAM Controller
100
102
104
DSLAM
116
122
118
Afe
120
Afe
Afe
Afe
Dsp
124
128
Svr
130
Internet
108
156
Afe
Afe
Afe
Afe
VDSL
Dsp
162
160
158
160
PSTN Voice Band
132
Switch
PSTN
150
100
112
114
106

FIG. 1

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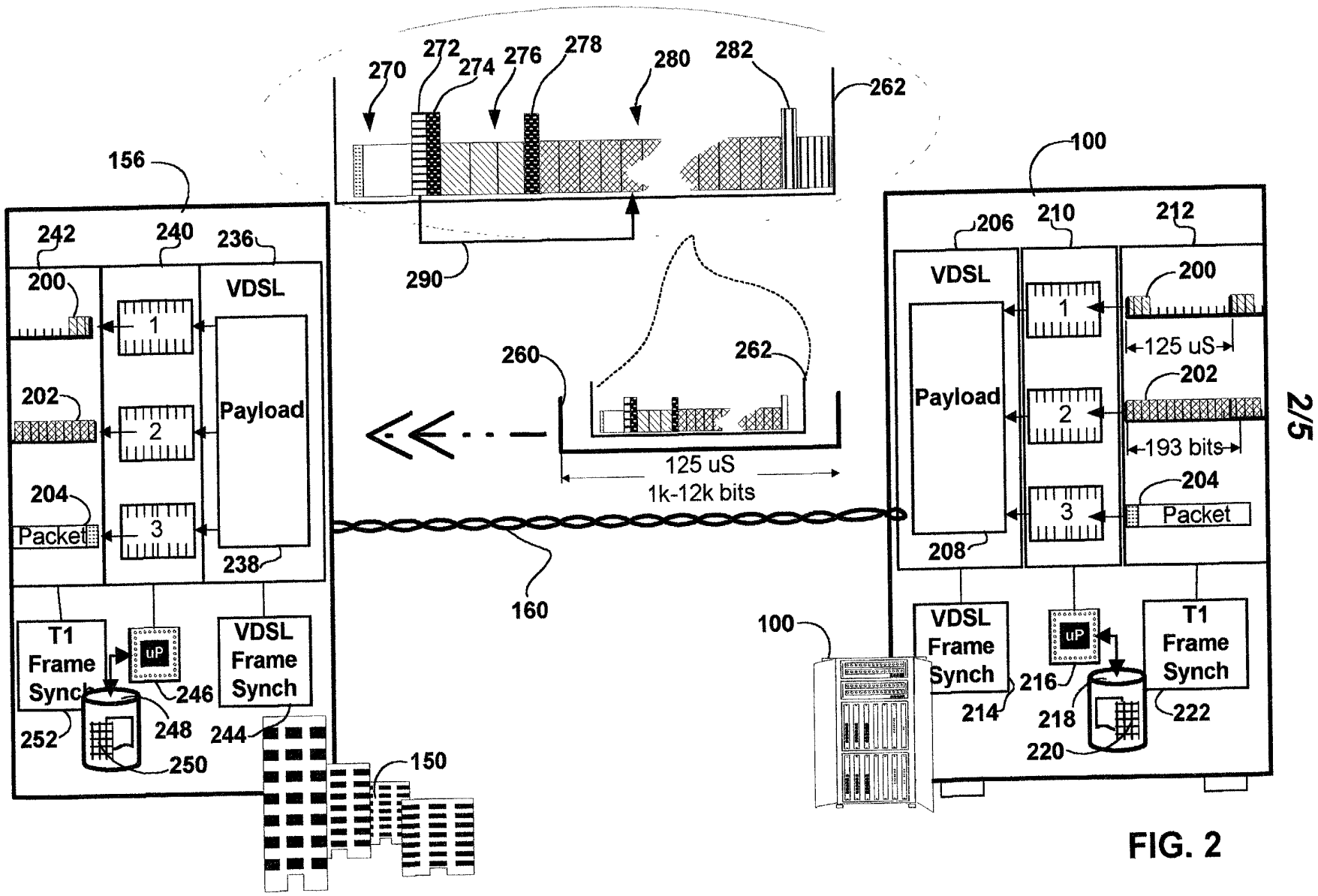
270
272
274
276
278
280
282
262
290
156
242
240
236
200
VDSL
1
202
2
Payload
204
Packet
3
238
260
262
125 uS
1k-12k bits
160
T1
Frame
Synch
uP
246
VDSL
Frame
Synch
252
248
244
250
150
100
206
210
212
VDSL
1
200
125 uS
Payload
2
202
193 bits
3
204
Packet
208
100
VDSL
Frame
Synch
uP
T1
Frame
Synch
216
214
218
222
220

FIG. 2

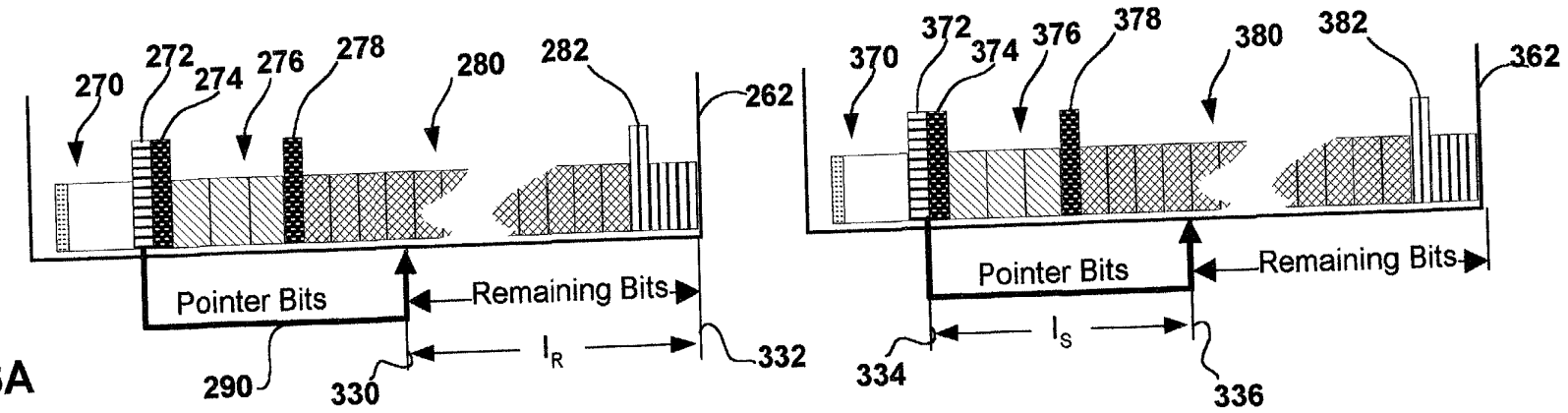
270
272
274
276
278
280
282
262
Pointer Bits
Remaining Bits
I_R
290
330
332
370
372
374
376
378
380
382
362
Pointer Bits
Remaining Bits
I_S
334
336

FIG. 3A

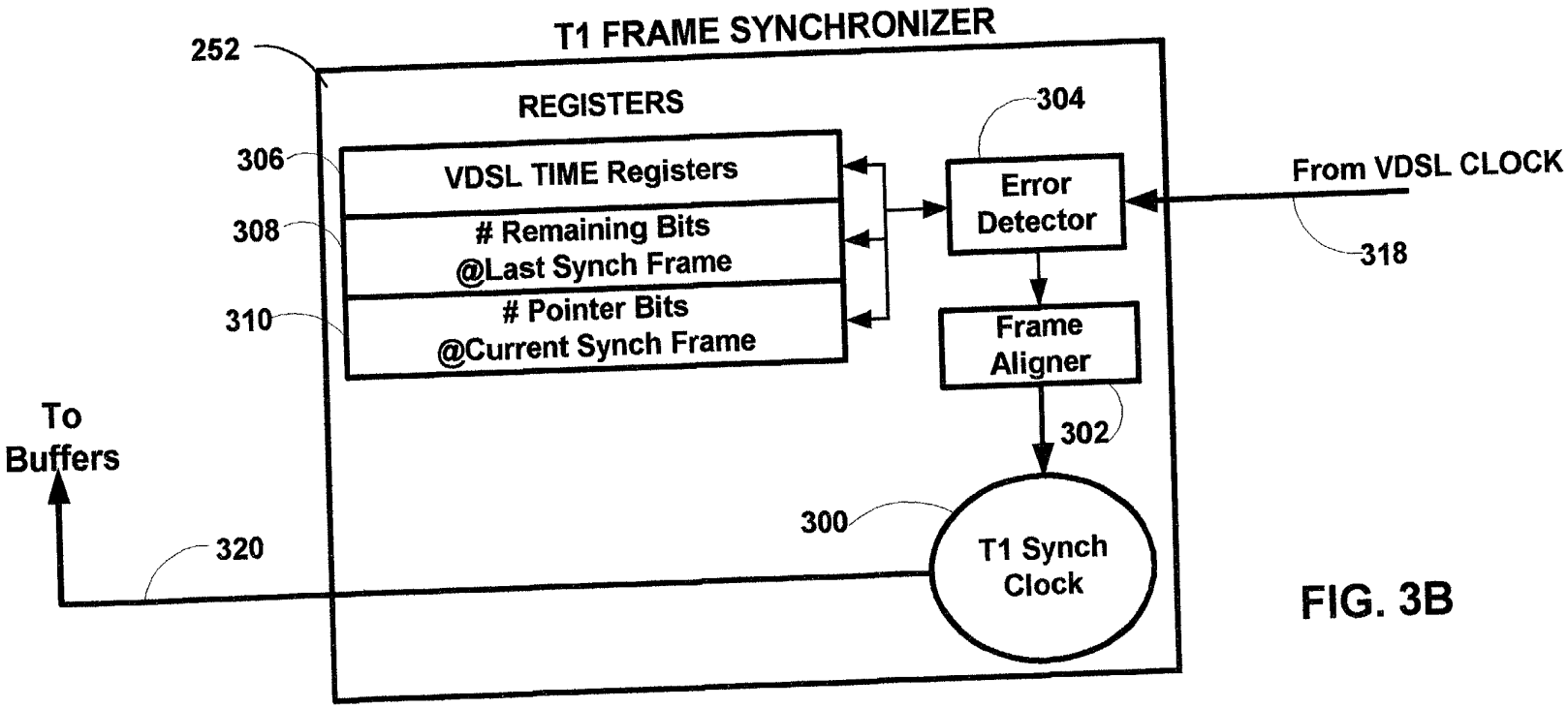
T1 FRAME SYNCHRONIZER
252
REGISTERS
304
306
VDSL TIME Registers
308
Remaining Bits
@Last Synch Frame
310
Pointer Bits
@Current Synch Frame
Error
Detector
From VDSL CLOCK
318
Frame
Aligner
302
To
Buffers
300
T1 Synch
Clock
320

FIG. 3B

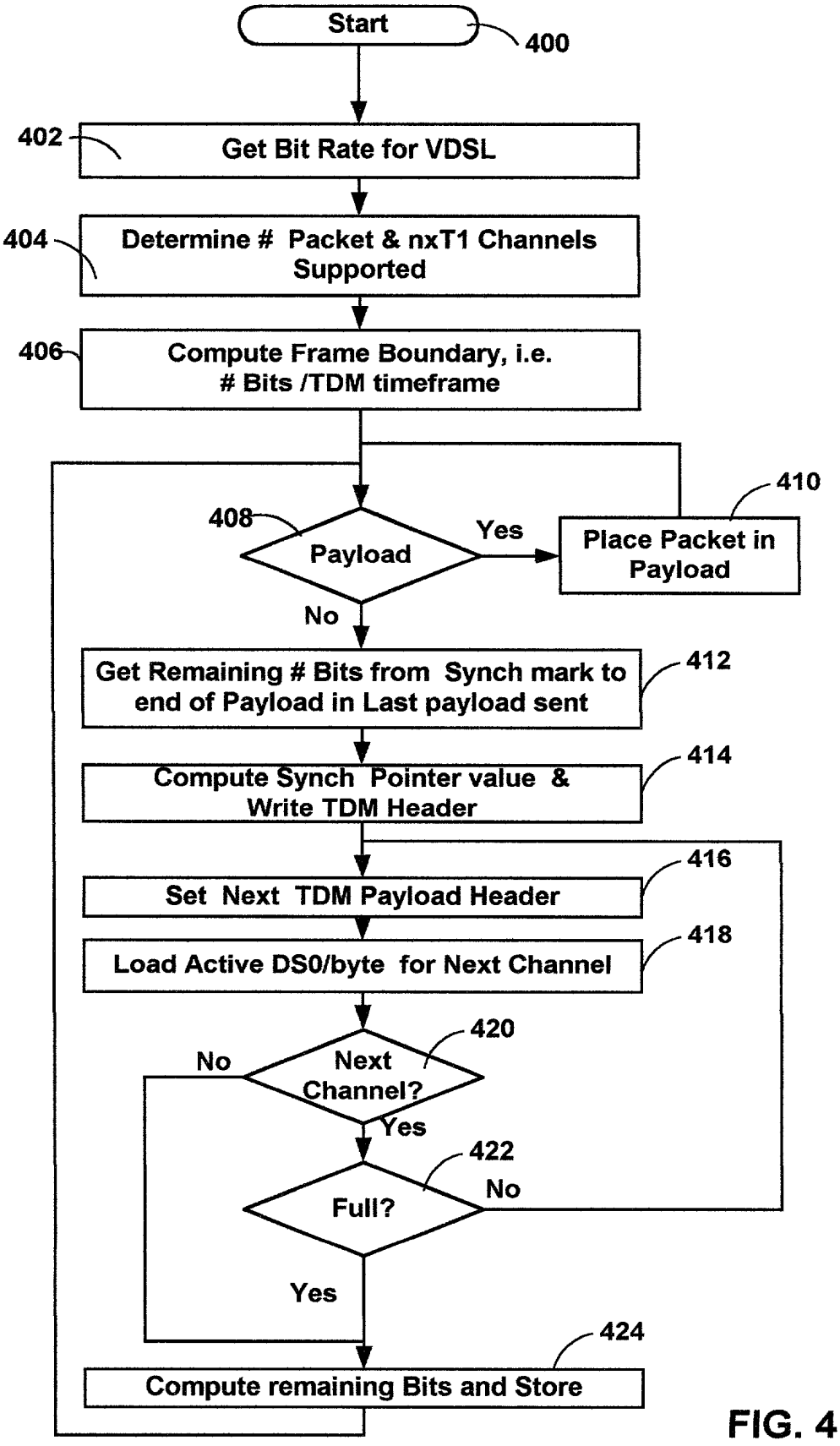

FIG. 4

Docket: 06-2750

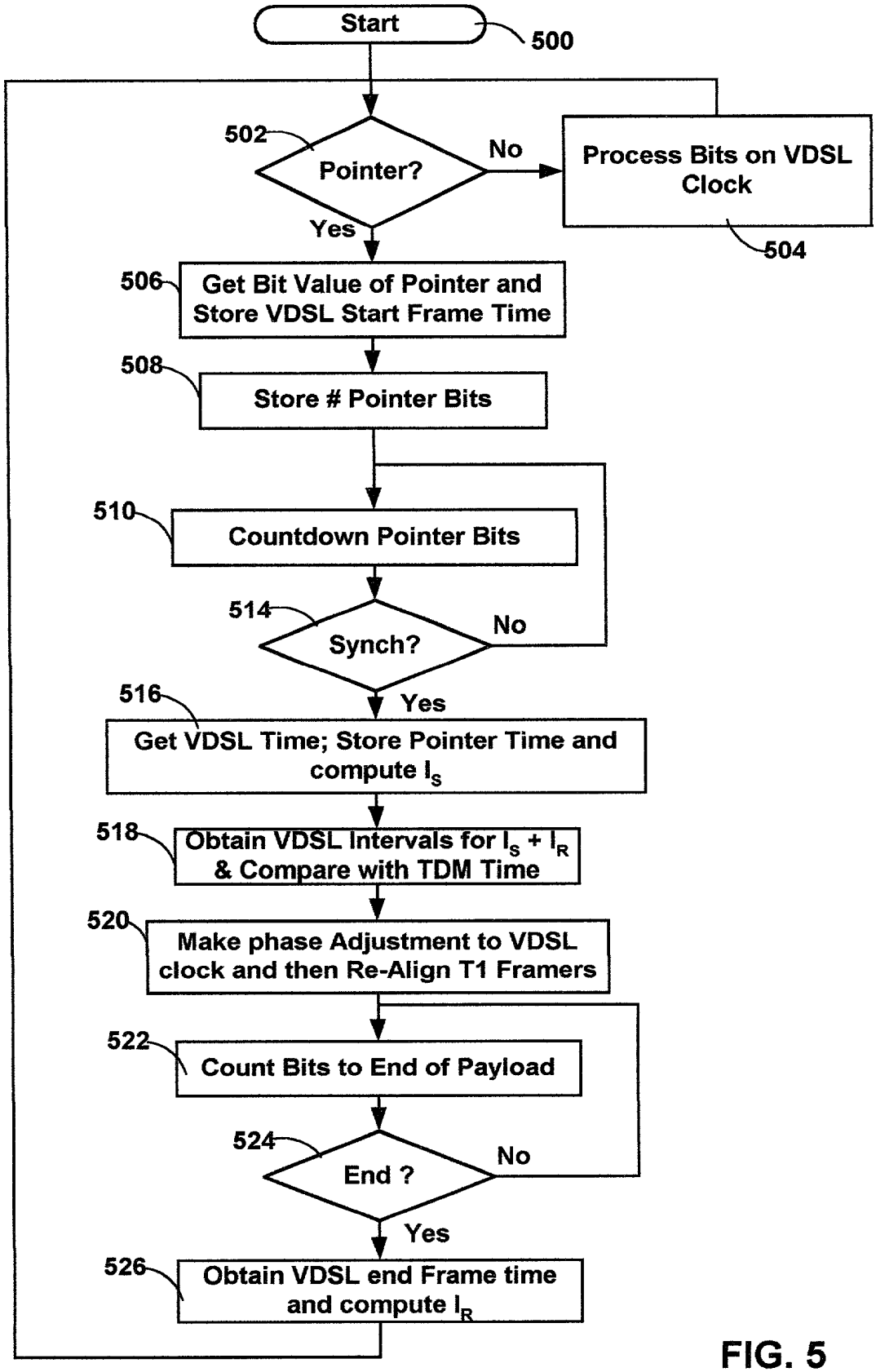

FIG. 5

Exhibit 1006, Page 5 of 5